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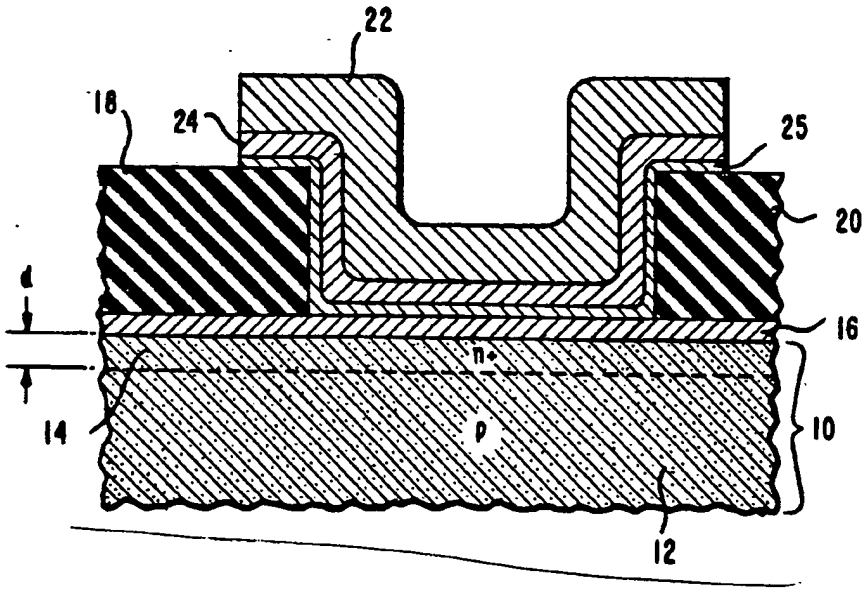
(54) Title: DIFFUSION BARRIER LAYER FOR INTEGRATED-CIRCUIT DEVICES



(57) Abstract

Titanium carbonitride has been discovered to be an effective diffusion barrier material for use in metallization structure for MOS integrated-circuit devices. A layer of the material (24) deposited under aluminum (22) prevents deleterious aluminum-silicon or aluminum-silicide interactions.

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DIFFUSION BARRIER LAYER FOR INTEGRATED-CIRCUIT DEVICES

Background of the Invention

This invention relates to integrated-circuit devices and, more particularly, to metallization structures used in devices of the metal-oxide-semiconductor (MOS) type.

In some metallization structures for MOS devices, it is known to utilize a diffusion barrier to prevent certain deleterious effects in the devices. Thus, for example, it is known to interpose a diffusion barrier between silicon (or a silicide) and an overlying aluminum layer to prevent silicon-aluminum or silicide-aluminum interactions. In that way, the likelihood is minimized that the metallization will cause harmful effects such as penetration and shorting of shallow junctions included in the devices.

Heretofore, as described in Journal of Applied Physics, Vol. 54, No. 6, June 1983, pp. 3195-3199, and Applied Physics Letters, Vol. 36, No. 6, March 15, 1980, pp. 456-458, materials such as titanium nitride or titanium carbide have been proposed for forming the aforementioned diffusion barrier layers in MOS devices. In practice, however, these materials have often been observed to exhibit characteristics such as cracking, peeling and poor step coverage which dictate against their inclusion in high-quality devices. Thus, a need exists for improved barrier layers.

Summary of the Invention

In accordance with this invention, an improved diffusion barrier layer is provided comprising titanium carbonitride. By way of example, the layer is formed in a chemical-vapor-deposition (CVD) process. Titanium carbonitride layers formed in this way exhibit excellent barrier properties and, moreover, are characterized by low stress, conformal step coverage and relatively low

resistivity.

Brief Description of the Drawing

The single-figure drawing, shows, in cross-section, a portion of an illustrative MOS integrated-circuit device embodying the present invention.

Detailed Description

The portion of a semiconductor device shown in the drawing comprises a silicon body 10 including a p-type silicon region 12 having a standard n^+-type source or drain region 14 formed therein. In some devices, the depth d of the p-n^+ junction is only about 1000-to-3000 Angstrom units (Å) below the surface of the body 10.

By way of example, a layer 16 of a standard refractory metal silicide is included on the body 10 overlying the source or drain region 14. Illustratively, the layer 16 is approximately 800-to-1000 Å thick and comprises cobalt silicide, tantalum silicide, titanium silicide, platinum silicide, palladium silicide, molybdenum silicide, or tungsten silicide. The use of such a silicide on silicon to achieve high-conductivity contacts and interconnects in MOS devices is well known.

Also shown is a conventional patterned dielectric layer of phosphorus-doped silicon dioxide comprising regions 18 and 20 each about 10,000 Å thick. High-conductivity contacts and interconnects are intended to be made through openings formed in the dielectric layer. In that way, electrical connections can be made to the source or drain region 14 and to other portions (not shown) of the device.

An electrical connection is made to the source or drain region 14 by a metallization structure that includes a patterned layer 22 that comprises a standard conductive material such as aluminum about 0.7-to-1 micrometer (μm)m thick. Interposed between the aluminum layer 22 and the silicide layer 16 is a diffusion barrier layer 24 made in accordance with the present invention.

Advantageously, the barrier layer 24 comprises titanium carbonitride that is formed, for example, in a chemical-vapor-deposition (CVD) step as described below. Illustratively, the layer 24 is approximately 1000 Å thick. Such a layer constitutes an effective barrier that prevents or substantially reduces silicon-aluminum and silicide-aluminum interactions in the depicted MOS device.

The titanium carbonitride layer 24 comprises a thermally stable, low-resistance material that is not harmfully affected by the relatively high temperatures and other processing conditions typically encountered in a conventional MOS device fabrication sequence. Moreover, the material exhibits good step coverage over underlying layers and is etchable by the same standard processes commonly employed to pattern aluminum.

The invention is useful in a variety of other structural arrangements.

Thus, for example, the layer 24 is also useful as a barrier in a structure in which the silicide layer 16 is replaced with a layer of tungsten. Additionally, the layer 24 is useful as a barrier in a structure in which the titanium carbonitride layer 24 is deposited directly on the surface of the silicon body 10 to form a barrier between the body 10 and the aluminum layer 22.

A diffusion barrier to aluminum may also be desirable where the underlying semiconductor material to be contacted comprises a relatively thick doped polysilicon layer. The herein-described titanium carbonitride material constitutes an advantageous material for such a purpose. Further, in a composite gate metallization structure comprising a silicide overlying doped polysilicon, a titanium carbonitride layer interposed between the silicide and the polysilicon is useful to prevent undesired diffusion of dopants from the polysilicon into the silicide layer.

In some cases, it is advantageous to interpose a conductive adhesion promoter between the barrier layer 24

and the region underlying the layer 24. By way of example, such an adhesion promoter layer 25 is shown in the drawing between the barrier layer 24 and the underlying layer 16. Illustratively, a 100-Å-thick layer of deposited titanium serves as an effective such adhesion promoter.

Illustratively, the starting material from which to form a titanium carbonitride layer comprises a known commercially available liquid designated $Ti[N(CH_3)_2]_4$. This liquid material, which is available in sealed ampule form from, for example, Alpha Products, Morton Thiokol, Inc., Danvers, Massachusetts, exhibits a relatively low vapor pressure under ambient conditions.

Preferably, the titanium carbonitride layer is formed in a CVD process. A low-resistance diffusion barrier layer thus formed on an integrated-circuit device is characterized by low stress and conformal step coverage.

The first step in a preferred CVD process is to load at least 25 grams of the aforespecified starting material into a container. By way of example, the surface area of the loaded material in the container should be at least about 50 square centimeters. Loading should be done in a controlled inert atmosphere (for example in a nitrogen or argon atmosphere) at room temperature with particular emphasis on avoiding any oxygen or moisture contamination of the starting material.

The loaded container is then connected via a conventional high-conductance valve to the entrance side of a standard three-zone CVD reactor that contains integrated-circuit chips on which a titanium carbonitride layer is to be deposited. Illustratively, the temperature in the reactor ranges from about 325 degrees Celsius at its entrance side to approximately 375 degrees Celsius at the exit or pump-down side thereof. The pressure in the reactor is established in the range of 40-to-100 milliTorr. A typical pumping speed is 150 cubic feet per minute.

Under these conditions, a titanium carbonitride layer forms on the chips in the reactor at a deposition rate of about 70-to-80 Å per minute. Effective barrier layers in the range of, for example, 1000-to-2000 Å are thus formed on the chips in a relatively short processing time.

A CVD-deposited layer of the type specified above may be designated TiC_xN_y. Analysis of such layers indicates that in many cases x and y are each equal to or approximately equal to 1. More generally, in such layers $0.8 < x < 1.2$ and $0.8 < y < 1.2$.

Significantly, titanium carbonitride layers are patternable in the same step in which an overlying layer of aluminum is etched. Thus, for example, a standard boron trichloride and chlorine plasma utilized to carry out conventional anisotropic reactive ion (or sputter) etching of aluminum is also effective to anisotropically etch the underlying titanium carbonitride layer.

Although the primary emphasis herein is on forming oxygen-free layers of titanium carbonitride, in some cases the unavoidable inclusion of some oxygen therein is tolerable and may even be desirable. Layers of oxygen-containing titanium carbonitride generally exhibit a higher resistance than titanium carbonitride but do have effective diffusion barrier properties. Layers containing up to 25 atomic percent oxygen exhibit acceptable resistivity for many device applications and therefore can be used.

Claims

1. An integrated-circuit device comprising first (22) and second (16) regions spaced apart from each other,

CHARACTERIZED BY

a diffusion barrier layer (24) comprising titanium, carbon and nitrogen interposed between said regions.

2. A device as in claim 1 wherein said barrier layer comprises titanium carbonitride.

3. A device as in claim 2 wherein said first region comprises a layer of aluminum overlying said barrier layer.

4. A device as in claim 3 wherein said second region comprises a layer of silicide.

5. A device as in claim 4 wherein said silicide is selected from the group consisting of cobalt silicide, tantalum silicide, titanium silicide, platinum silicide, palladium silicide, molybdenum silicide, and tungsten silicide.

6. A device as in claim 3 wherein said second region comprises a layer of tungsten.

7. A device as in claim 3 wherein said second region comprises a silicon body (10) having a shallow $p\text{-}n^+$ junction formed below the surface thereof.

8. A device as in claim 1 wherein said barrier layer comprises a CVD-deposited layer of titanium carbonitride.

9. A device as in claim 8 wherein said barrier layer is 1000-to-2000 Å thick.

10. A device as in claim 1 wherein said barrier layer comprises partially oxidized titanium carbonitride.

11. A device as in claim 10 wherein said second region comprises a layer (25) of conductive adhesion promoter directly underlying and in contact with said barrier layer.

12. A device as in claim 11 wherein said

adhesion promoter layer comprises titanium.

13. A method of making an integrated-circuit device of the type that includes first and second regions having a diffusion barrier layer interposed therebetween, said method characterized by the steps of

forming on said second region by chemical vapor deposition a diffusion barrier layer that comprises titanium, carbon and nitrogen,

and then forming said first region overlying said barrier layer.

14. A method as in claim 13 wherein said barrier layer comprises titanium carbonitride.

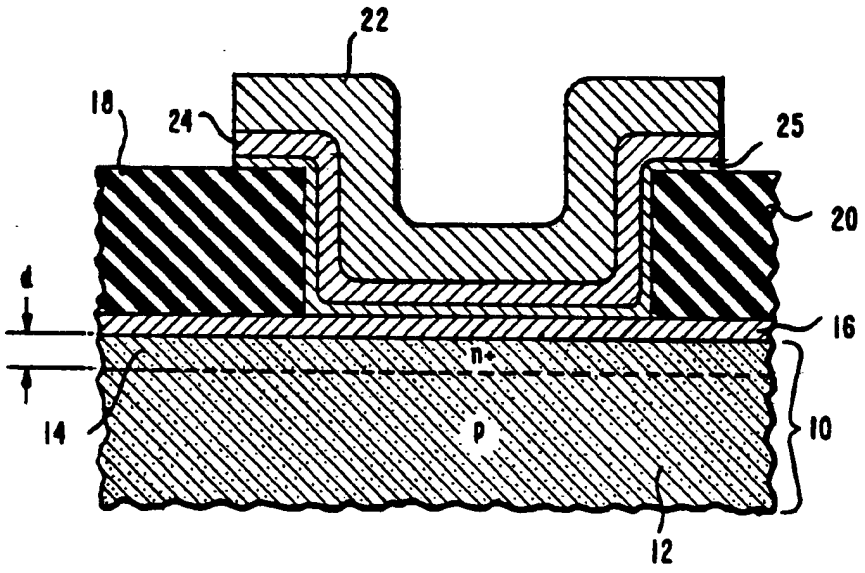
15. A method as in claim 14 wherein said first region comprises a layer of aluminum.

16. A method as in claim 15 comprising the additional step of correspondingly patterning said aluminum and titanium carbonitride layers.

17. A method as in claim 16 wherein said aluminum and titanium carbonitride layers are sequentially etched by the same etchant.

18. A method as in claim 17 wherein said etchant comprises a plasma derived from boron trichloride and chlorine.

19. A method as in claim 13 wherein said barrier layer comprises partially oxidized titanium carbonitride.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INTERNATIONAL SEARCH REPORT

International Application No PCT/US 85/01292

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 23/48

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System [8]	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [9]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	IBM Technical Disclosure Bulletin, volume 25, nr. 12, May 1983, New York, (US) C.Y. Ting:"New structure for contact metallurgy", pages 6398-6399 see page 6398, paragraph 2	1,3-5
A	Journal of Applied Physics, volume 54, nr. 6, June 1983, New York, (US) M. Eizenberg et al.:"Interaction of reactively sputtered titanium carbide thin films with Si,SiO2, Ti,TiSi$_2$ and Al", pages 3195-3199, see introduction (cited in the application)	1,3-5
A	US, A, 3906540 (B.E. HOLLINS, NAT. SEMICONDUCTOR) 16 September 1975, see claims 1-3	1,3-5

* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
27th September 1985	31 OCT 1985
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	G.L.M. Kruydenberg

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ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 85/01292 (SA 10187)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 14/10/85

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 3906540	16/09/75	None	